REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 through 11 and 54 through 56 are now in this case. Claims 1 through 11 are amended. Claims 12 through 53 are canceled Claims 54 through 56 are added.

Claims 12 through 42 were previously withdrawn from consideration as directed to a non-elected invention, and are now canceled. Claims 43 through 53 are canceled because they became superfluous considering the amendment to claim 1 presented in this paper.

The specification is amended, on page 1, to update the serial numbers of the patent applications that were copending at the time of filing this application.

The specification is also amended, on page 6, to include additional nomenclature that distinguishes between two disclosed constituent layers of the top electrode. This nomenclature corresponds to the amendment to claim 11 and to new claim 54, as will be discussed below. No new matter is presented by this amendment to the specification, because the amendment only adds the distinguishing labels of "first layer 100" and "strap layer 110".

Claims 1 through 11 and 43 through 53 were rejected under §103 as unpatentable over the Block et al. reference[1] in view of the Doan et al. reference[2]. The Examiner asserted that the Block et al. reference discloses each element of claims 1, 11, and 43, except for the sidewalls.[3] The Examiner asserted that the Doan et al. reference discloses sidewalls 112 positioned at a perimeter of a top metal level capacitor,[4] and that it would have been obvious to modify the

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[1] U.S. Patent No. 6,737,728 B1, issued May 18, 2004 to Block et al., filed October 12, 2000.
[2] U.S. Patent No. 6,303,953 B1, issued October 16, 2001 to Doan et al., filed January 29, 1999 as a divisional of U.S. Patent No. 6,048,763 filed August 21, 1997.
[3] Office Action of May 25, 2004, page 3.
[4] *Id., citing* Doan et al., *supra*, Figure 1.

capacitor of the Block et al. reference according to Doan et al.'s teachings to provide an improved structure for fabrication of a high value capacitor.[5]

Claim 1 is amended to more completely cover all aspects of Applicants' invention, and to clarify its patentability over the applied references.

Amended claim 1 is now directed to an integrated circuit including a top metal level capacitor, in which a plurality of levels of metal conductors are expressly recited, and in which a top metal level is defined as that which is disposed furthest from that a surface of a semiconductor substrate.[6] Amended claim 1 is further amended to recite dielectric sidewall structures disposed adjacent to the bottom electrode and at least a portion of the capacitor dielectric,[7] and that the top electrode is disposed over the capacitor dielectric and extends over at least one of the dielectric sidewall structures to conductively contact a second conductor in the top metal level.[8] Because of the clear support in the specification for this amendment to claim 1, Applicants submit that no new matter is presented by the amendment to claim 1.

Claims 2 through 10 are amended for consistency with the amendment to claim 1, and also for clarity in the case of claim 9.

The structure of amended claim 1 and its dependent claims provides important advantages over the prior art. Specifically, the inventive integrated circuit of these claims includes a top metal level capacitor that, because it connects to conductors in the top metal level, can be made to a sufficiently large size that it can serve as a decoupling capacitor.[9] In addition, because the capacitor is formed over the top metal level, its construction is not dependent on subsequent metal processes and therefore is readily compatible with conventional packaging technology of any type.[10] And the sidewall structures of the capacitor

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[5] *Id.*
[6] *See* specification of application S.N. 10/669,847 at page 4, lines 12 through 19.
[7] *See* specification, *supra,* at page 9, lines 1 through 15.
[8] *See* specification, *supra,* page 6, line 1 through page 7, line 2; page 9, line 17 through page 10, line 15; Figures 1A, 1B, 2L
[9] Specification, *supra,* page 4, line 21 through page 5, line 5; page 6, lines 13 through 19.
[10] Specification, *supra,* page 5, lines 7 through 11.

facilitate the fabrication of this capacitor with minimal risk of shorting between the top and bottom electrodes.[11]

Applicants respectfully submit that amended claim 1 and its dependent claims are all patentably distinct over the prior art of record in this case, on the grounds that the teachings of the applied references cannot be properly combined in such a manner as to reach the claims.

First, Applicants agree with the Examiner that the Block et al. reference fails to disclose the dielectric sidewall structures of amended claim 1. Applicants submit, however, that the Block et al. reference also fails to disclose a capacitor having a bottom electrode that is positioned over the top metal level (and therefore having a capacitor dielectric and a top electrode also disposed over the top metal level). As is now recited in amended claim 1, the top metal level is recited as being the one of the plurality of levels of metal conductors that is disposed furthest from the surface of the substrate at which the levels are disposed. In contrast, however, the capacitors disclosed in the Block et al. reference are each disposed beneath a metal level; in other words, the metal level over which the bottom electrode of the Block et al. capacitor is disposed is not the top metal level (there is another metal level overlying that metal level). Specifically, Figures 1 and 2 of the Block et al. reference shows a metal level including conductors 101, 102, 108 disposed over capacitor 100,[12] and Figure 4 of the Block et al. reference shows a metal level including conductor 101 disposed over capacitor 100.[13]

Applicants further submit that the teachings of the Doan et al. reference cannot be properly combined with those of the Block et al. reference so as to reach amended claim 1. First, the structure having the sidewalls 112 in the Doan et al. reference is not a capacitor, but rather is a gate structure for a MOS transistor to be used as a word line device.[14] Second, the alleged "capacitor" in the Doan et al. reference is nowhere near the top metal level; rather, the Doan et al. reference clearly contemplates many conductor levels above that of the gate structure and

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[11] Specification, *supra*, page 6, line 21 through page 7, line 2.
[12] Block et al., *supra*, column 4, lines 41 through 67.
[13] Block et al., *supra*, column 5, lines 15 through 30.
[14] Doan et al., *supra*, column 5, lines 48 through 67.

sidewalls 112. [15] At best, therefore, Applicants submit that the Doan et al. reference would suggest that transistors in the Block et al. structure (disposed well below its capacitors[16]) are to have their gate structures constructed as taught by Doan et al. There is simply no suggestion from the Doan et al. reference that its sidewall structures are to be applied to a capacitor, much less a capacitor having its bottom plate above that of the top metal level, as claimed.

This lack of suggestion to apply the sidewalls of the Doan et al. reference to any capacitor is especially made evident from the stated reasons for these sidewall structures in the reference itself. The Doan et al. reference expressly states that sidewall spacers 112 "protect the word lines 102 from the etchants used to expose the active area", and "act as a shield during the various implantation steps to prevent dopant atoms from entering a channel region"[17]. These functions are simply not applicable to the capacitor of Block et al., considering that there is no etch to expose active regions after formation of that capacitor, and that there is no subsequent ion implantation step (*e.g.*, source/drain implant) applied to that capacitor that can possibly affect the channel region. The Doan et al. reference does mention that sidewall spacers 112 also provide electrical isolation between the gate electrode 108 and the active area 110;[18] however, this is also not a concern in the Block et al. capacitor, considering that the bottom plate of the Block et al. capacitor is already isolated from the active regions of the substrate, is disposed in contact with an underlying conductor (102) and an underlying insulator (110).[19]

For these reasons, Applicants submit that there is no suggestion from the prior art to combine the Block et al. and Doan et al. references in such a manner as to reach amended claim 1. The important advantages provided by the integrated circuit of the claims, which are directly due to the differences between the claims and the prior art, further support the patentability of these claims.

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[15] *See* Doan et al., *supra*, column 9, lines 52 through 54.
[16] Block et al., *supra*, column 3, line 66 through column 4, line 2 (referring to the implementation of its capacitor in the "back-end of a semiconductor manufacturing process").
[17] Doan et al., *supra*, column 5, lines 56 through 62.
[18] Doan et al., *supra*, column 5, lines 63 through 65.
[19] *See* Block et al., *supra*, Figure 1.

Accordingly, Applicants respectfully submit that amended claim 1 and its dependent claims are patentably distinct over the prior art of record in this case.

Claims 54 through 56 are added to more completely cover all aspects of Applicants' invention. Claim 54 further requires, relative to claim 1 upon which it depends, that the top electrode is comprised of a first layer that is disposed over and adjacent to the capacitor dielectric, and a conductive strap that is disposed over and in contact with the first layer, and extends over a dielectric sidewall structure to the second conductor of the top metal level.[20] Claim 55 further requires, relative to claim 54 upon which it depends, that the conductive strap comprises a diffusion barrier material.[21] And claim 56 further requires, relative to claim 54 upon which it depends, that the dielectric sidewall structures are also disposed adjacent to at least a portion of the first layer of the top electrode.[22] Because of the clear support for these new claims, Applicants submit that no new matter is presented by the addition of claims 54 through 56.

For the same reasons as discussed above relative to claim 1, Applicants respectfully submit that new claims 54 through 56 are also patentably distinct over the prior art applied against the claims.

Applicants also respectfully submit that claim 54 and its dependent claims 55 and 56 are even further patentably distinct over the prior art. The construction of the top electrode recited in new claim 54 is nowhere shown by either of the Block et al. and Doan et al. references, and therefore the combined teachings of these references fall even further short of these claims than they do (properly combined) of amended claim 1. For this additional reason, Applicants submit that new claims 54 through 56 are patentably distinct over the prior art of record in this case.

As mentioned above, independent claim 11 was also rejected under §103 as unpatentable over the Block et al. and Doan et al. references. Claim 11 is also amended to more

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[20] *See* specification, *supra*, page 6, lines 1 through 11.
[21] *Id.*
[22] *See* specification, *supra*, at page 9, lines 8 through 15.

completely cover all aspects of Applicants' invention, and to clarify its patentability over the applied references.

Similarly to amended claim 1, amended claim 11 is now directed to an integrated circuit including a top metal level capacitor. The top metal level is defined, in amended claim 11, as the one of a plurality of levels of metal conductors that is disposed furthest from that a surface of a semiconductor substrate.[23] And as in amended claim 1, amended claim 11 recites dielectric sidewall structures that are disposed adjacent to the bottom electrode and at least a portion of the capacitor dielectric.[24] Amended claim 11 further recites that the top electrode comprises a first layer comprised of TiN disposed over and in contact with the capacitor dielectric, and a strap layer comprised of TaN that extends over at least one of the dielectric sidewall structures to conductively contact a second conductor in the top metal level.[25] Applicants submit that no new matter is presented by this amendment to claim 11, considering the clear support for these elements in the specification.

The structure claimed in amended claim 11 provides similar advantages as discussed above relative to amended claim 1, such advantages including a top metal level capacitor that, because it connects to conductors in the top metal level, can be made to a sufficiently large size capable of being a decoupling capacitor[26] and can be made of materials that can be selected without constraints of subsequent metal processes,[27] and that has minimal risk of shorting across the electrodes.[28]

For the same reasons as discussed above relative to amended claim 1, Applicants respectfully submit that amended claim 11 is patentably distinct over the Block et al. and Doan et al. references.

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[23] *See* specification of application S.N. 669,847 at page 4, lines 12 through 19.
[24] *See* specification, *supra*, at page 9, lines 1 through 15.
[25] *See* specification, *supra*, page 6, line 1 through page 7, line 2; page 9, line 17 through page 10, line 15;. Figures 1A, 1B, 2I.
[26] Specification, *supra*, page 4, line 21 through page 5, line 5; page 6, lines 13 through 19.
[27] Specification, *supra*, page 5, lines 7 through 11.
[28] Specification, *supra*, page 6, line 21 through page 7, line 2.

In summary, Applicants respectfully submit that there is no suggestion to modify the teachings of the Block et al. reference with those of the Doan et al. reference to arrive at a capacitor having both of its bottom and top electrodes positioned over the top metal level in the integrated circuit, and having dielectric sidewall structures disposed adjacent to the bottom electrode and the capacitor dielectric, much less over which a strap layer of the top capacitor electrode extends, as claimed.

This lack of suggestion is evident considering that the structure of the Doan et al. reference associated with alleged sidewalls 112 is not a capacitor, but rather the gate electrode of a word line transistor[29] that is nowhere near the top metal level of the Doan et al. structure.[30] To the extent that suggestion does exist to modify the teachings of the Block et al. reference with the Doan et al. reference, this combination would simply result in lower level transistors in the Block et al. structure (disposed well below its capacitors[31]) having their gate structures constructed (with sidewalls 112) as taught by Doan et al. There is simply no suggestion from the Doan et al. reference that its sidewall structures are to be applied to a capacitor, much less a capacitor having its bottom plate above that of the top metal level, as claimed.

As discussed above relative to amended claim 1, while the Doan et al. reference may provide motivation to use its sidewall structures in connection with a lower level transistor gate structure,[32] none of those reasons in any way apply to the fabrication of a capacitor above the top metal level, as required by the claims. Accordingly, these references provide no motivation to combine their teachings in such a manner as to reach amended claim 11.

For these reasons, and also considering the important advantages of the integrated circuit of amended claim 11 over conventional structures, Applicants submit that there is no suggestion from the prior art to combine the Block et al. and Doan et al. references in such a

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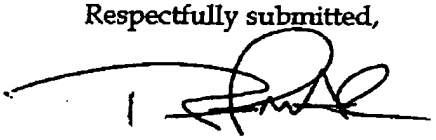
[29] Doan et al., *supra*, column 5, lines 48 through 67.
[30] *See* Doan et al., *supra*, column 9, lines 52 through 54.
[31] Block et al., *supra*, column 3, line 66 through column 4, line 2 (referring to the implementation of its capacitor in the "back-end of a semiconductor manufacturing process").
[32] Doan et al., *supra*, column 5, lines 56 through 65.

manner as to reach amended claim 11. Accordingly, Applicants respectfully submit that amended claim 11 is patentably distinct over the prior art of record in this case.

The references cited by the Examiner but not applied have been considered, but are not felt to come within the scope of the claims now in this case.

For these reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,



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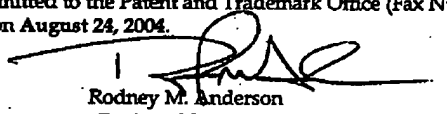

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